IN THE SPECIFICATION

Please replace paragraph 0040 with the following amended paragraph:

[0040] Referring to Figure 7, a system 100 for generating several types of pseudorandom sequences is shown. As with the embodiment shown in Figure 2, the system 100 includes a bit position counter 12, a multiplexer 14, a spreading factor selector 16, a bit by bit AND gate 18, an index selector 20, and an XOR gate 22. However, this embodiment includes a mode switch 60 which switches between a first mode for generating OVSF codes and a second mode for generating Hadamard codes. When the mode selection switch 60 is in a first position, the system 100 operates in the manner identical to the system 10 shown in Figure 2, whereby the multiplexer 14 reverses the bit order of the bit output from the bit position counter 12. However, when the mode switch 60 is in a second position, the reordering of the bits is not performed by the multiplexer 14 and the bits are passed directly through the multiplexer 14 to the bit by bit AND gate 18. This is shown in Figure 8 whereby the straight dotted lines through the multiplexer 14 illustrate the bits being passed directly through the multiplexer 14 without being reordered.

Please replace paragraph 0042 with the following amended paragraph:

[0042] The same ANDing and XORing process is performed as was described with reference to the generation of the OVSF codes, except that the bits from the

counter 12 are not reversed. This results in an output from the system 100 of 0, 1, 1, 0, 0, 1, 1, 0. This correctly matches the fourth leg of the Hadamard code prestructure shown in Figure 6. These outputs may be optionally mapped whereby an output of 1 is mapped to minus 1 and an output of 0 is mapped to 1.